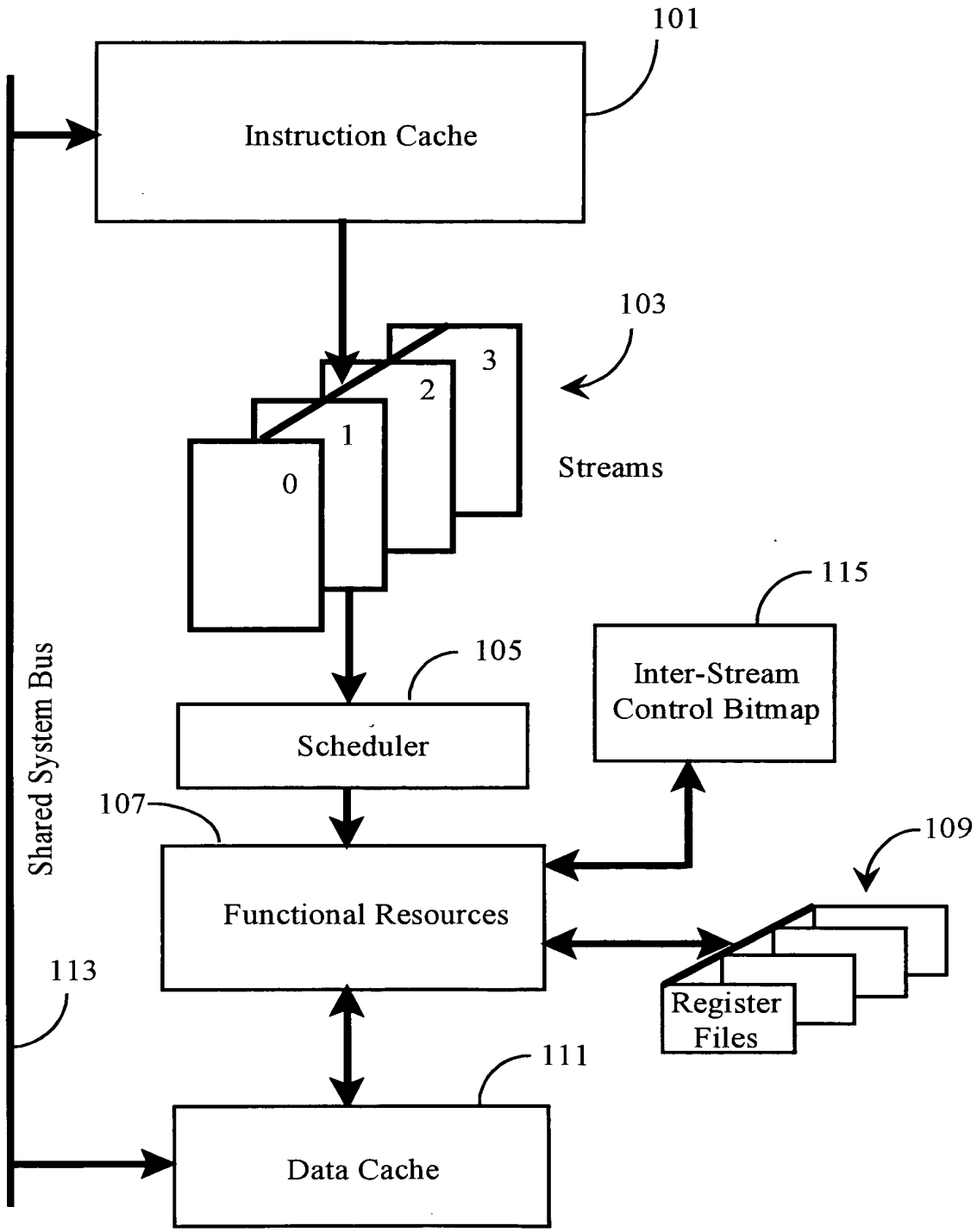
101
Instruction Cache
103
3
2
1
0
Streams
115
Inter-Stream
Control Bitmap
105
Scheduler
107
Functional Resources
109
Register
Files
113
Shared System Bus
111
Data Cache

*Fig. 1A*

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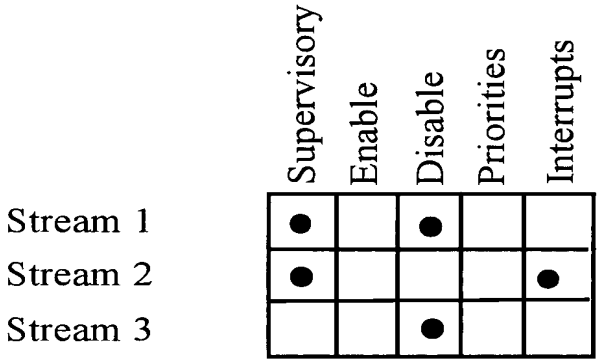
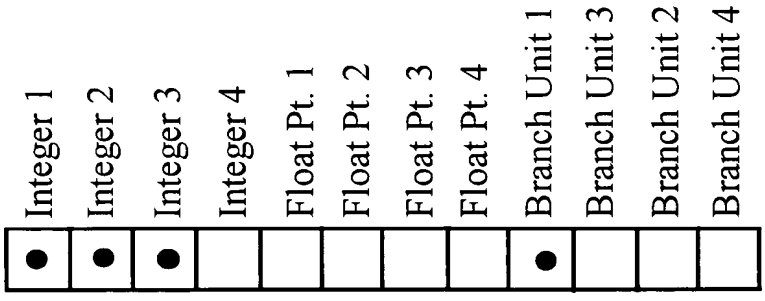



Control Authorization for Stream 0

***Fig. 1B***




Hard Resource Assignment for Stream 0

***Fig. 1C***

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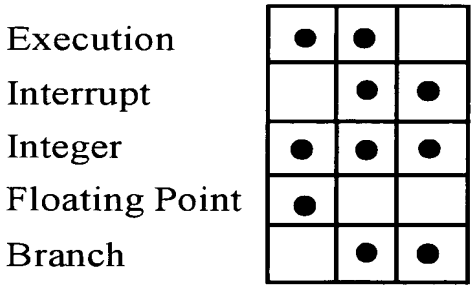


Priorities for Stream 0

***Fig. 1D***

Control Indicators for Stream 0

***Fig. 1E***

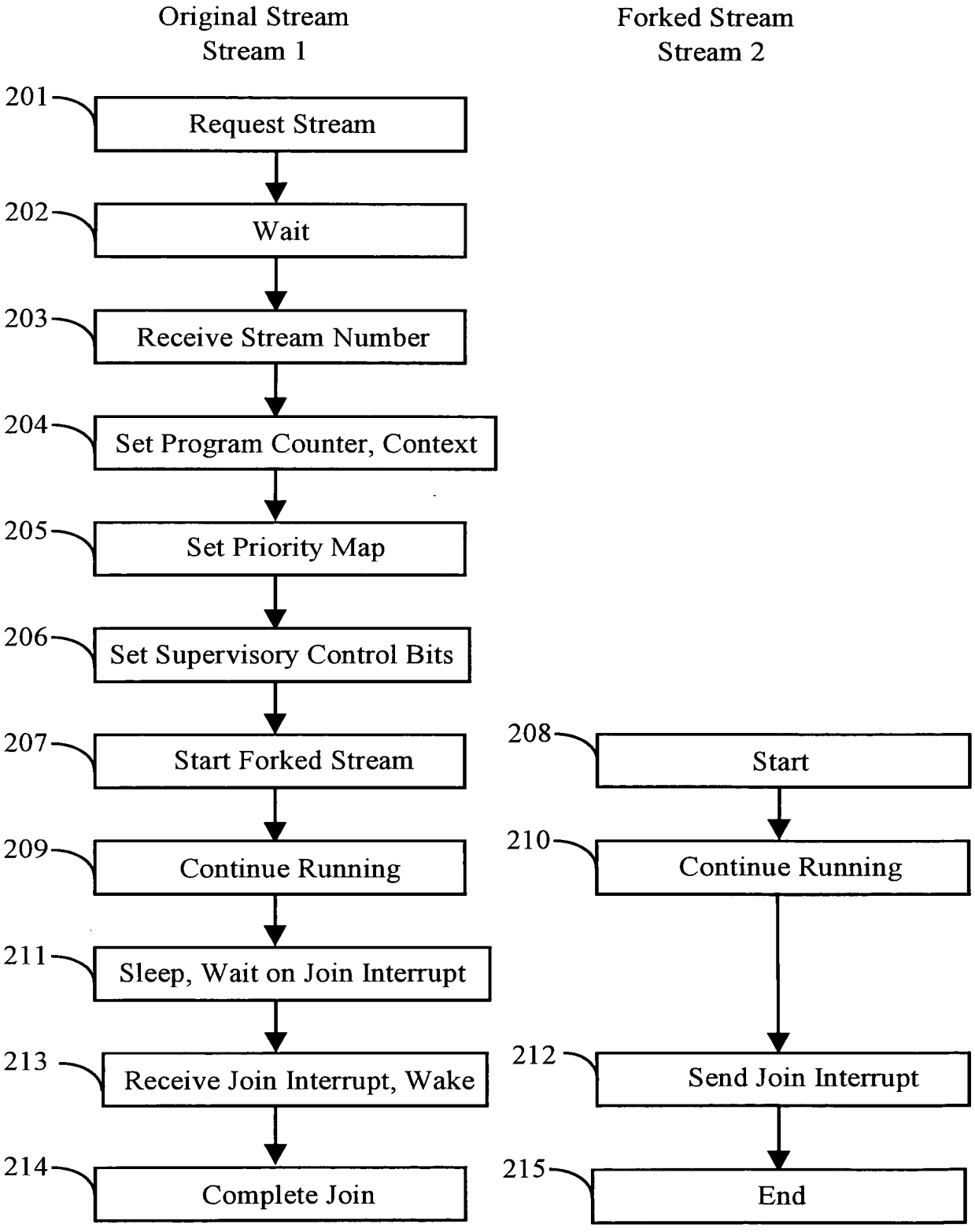
Original Stream
Stream 1
Forked Stream
Stream 2
201
Request Stream
202
Wait
203
Receive Stream Number
204
Set Program Counter, Context
205
Set Priority Map
206
Set Supervisory Control Bits
207
Start Forked Stream
208
Start
209
Continue Running
210
Continue Running
211
Sleep, Wait on Join Interrupt
213
Receive Join Interrupt, Wake
212
Send Join Interrupt
214
Complete Join
215
End

*Fig. 2A*

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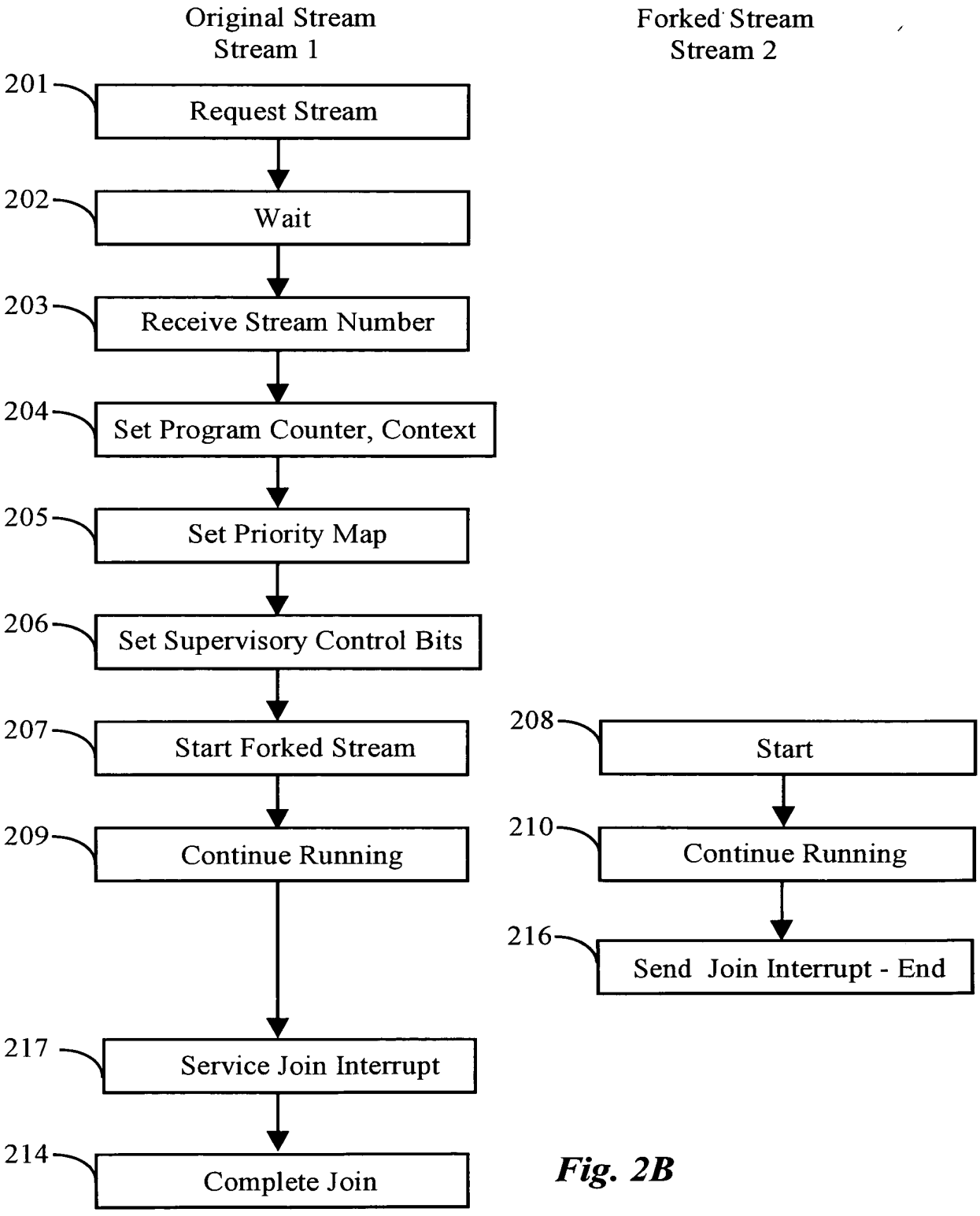


*Fig. 2B*

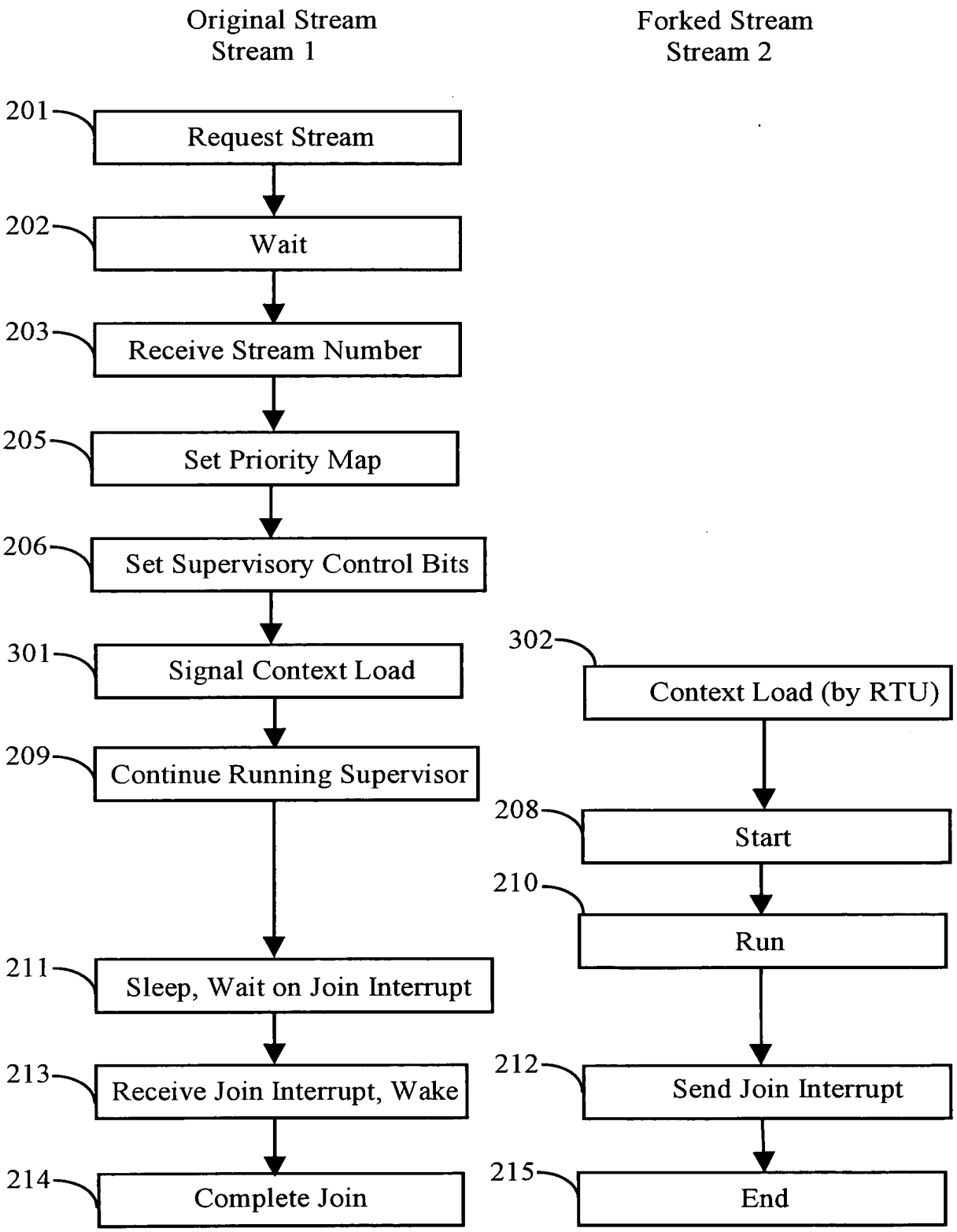
Original Stream
Stream 1
Forked Stream
Stream 2
201
Request Stream
202
Wait
203
Receive Stream Number
205
Set Priority Map
206
Set Supervisory Control Bits
301
Signal Context Load
209
Continue Running Supervisor
211
Sleep, Wait on Join Interrupt
213
Receive Join Interrupt, Wake
214
Complete Join
302
Context Load (by RTU)
208
Start
210
Run
212
Send Join Interrupt
215
End

*Fig. 3*

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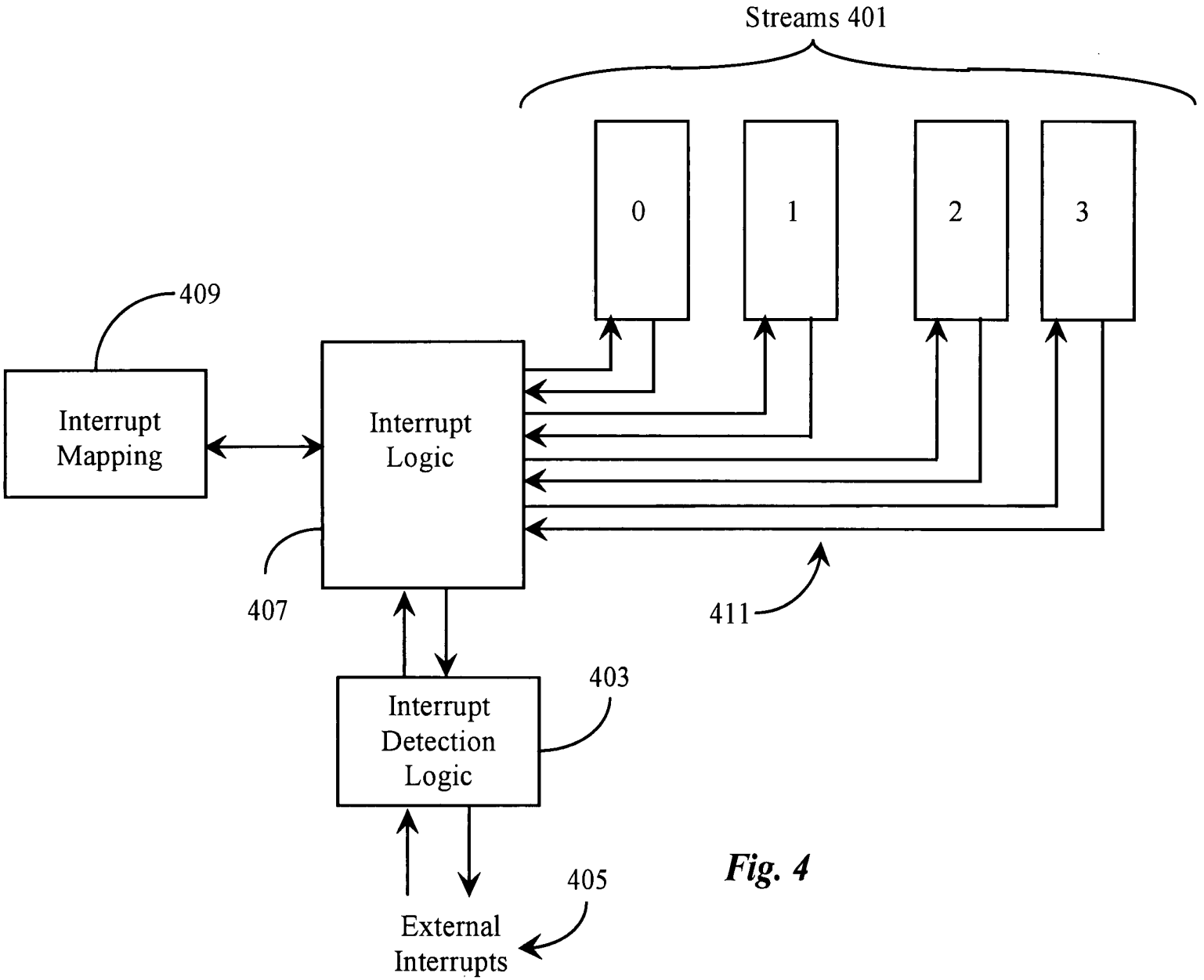


*Fig. 4*

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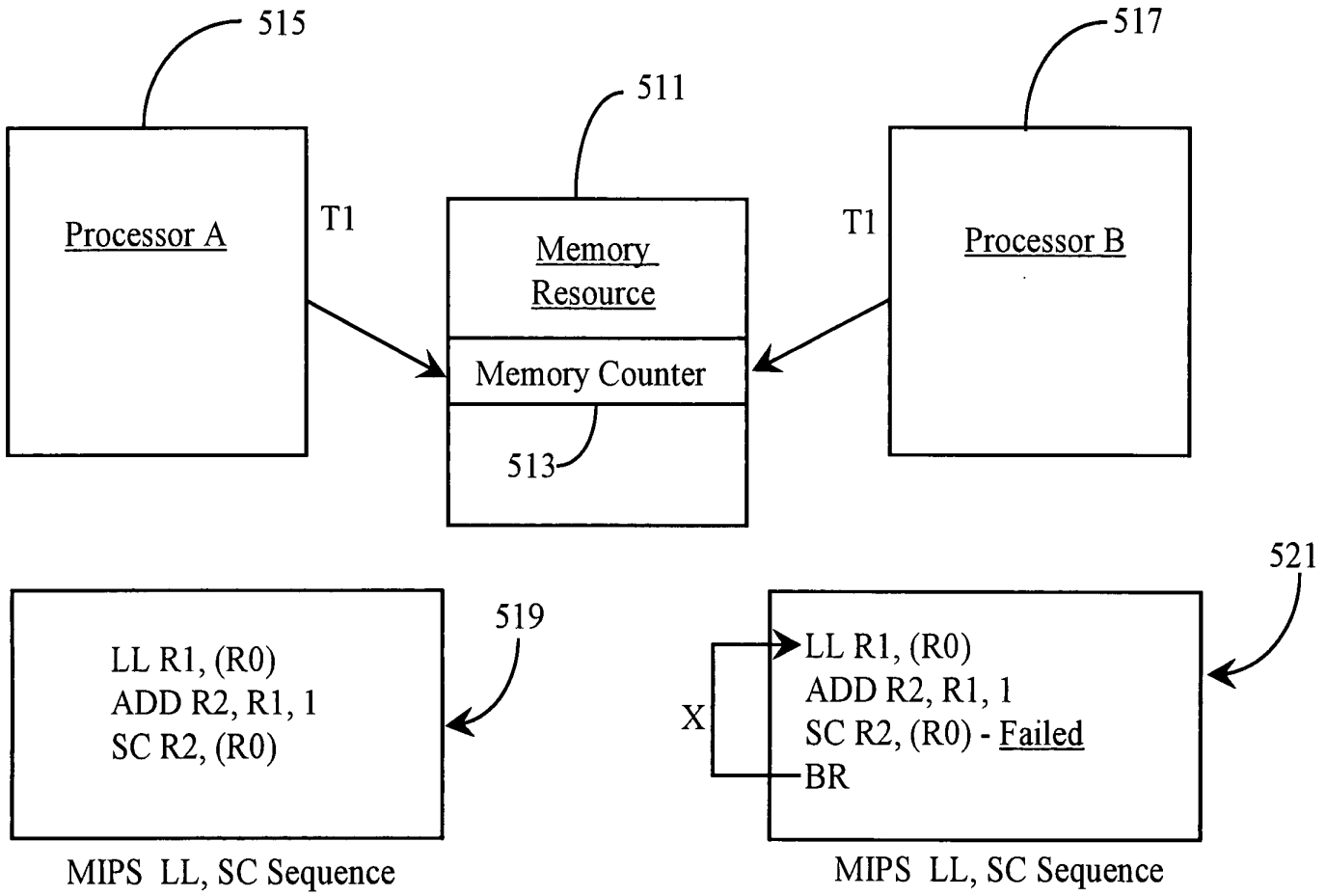


*Fig. 5 (Prior Art)*

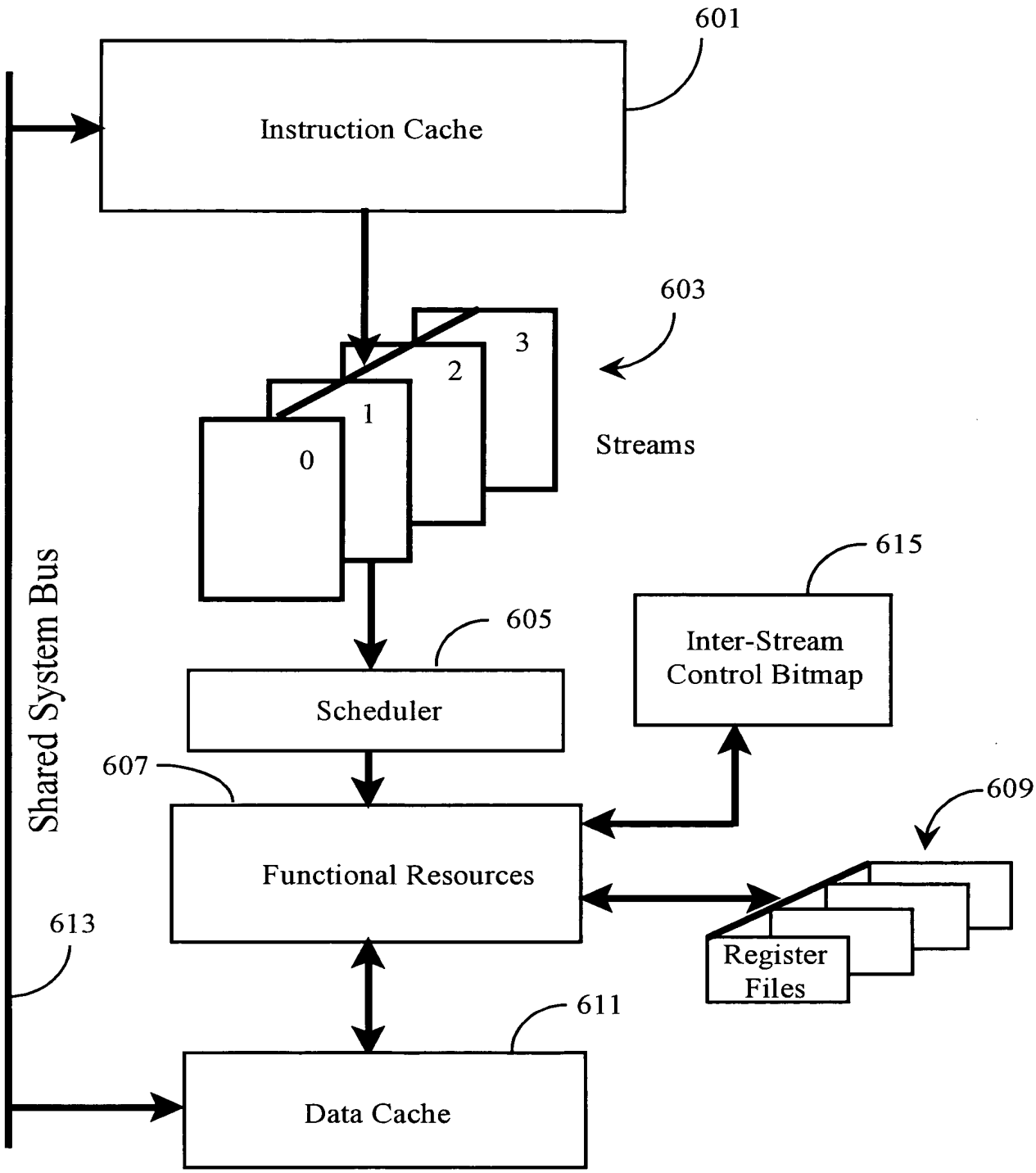
601
Instruction Cache
603
3
2
1
0
Streams
615
Inter-Stream
Control Bitmap
605
Scheduler
607
609
Functional Resources
Register
Files
613
611
Data Cache
Shared System Bus

*Fig. 6*

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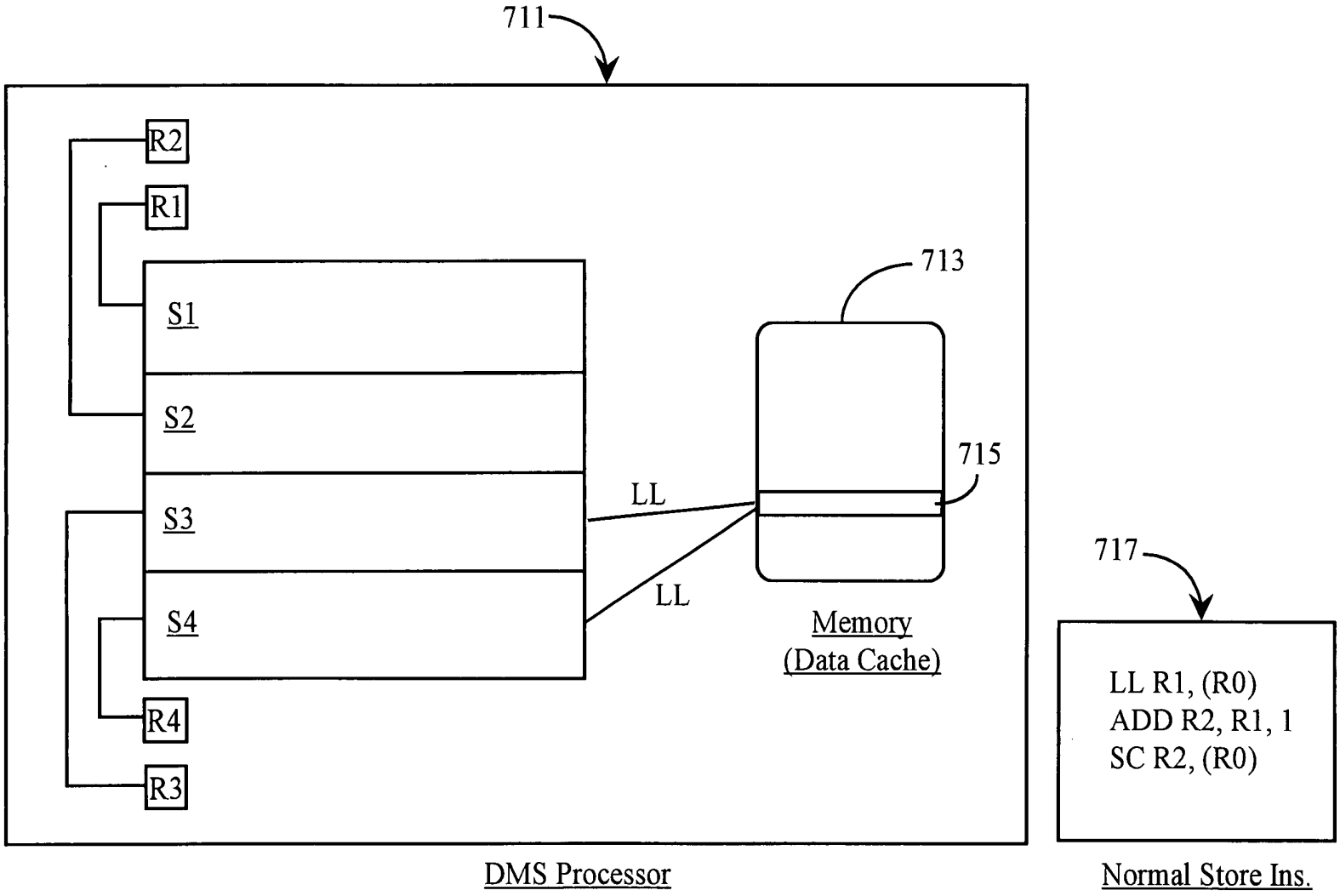


*Fig. 7*

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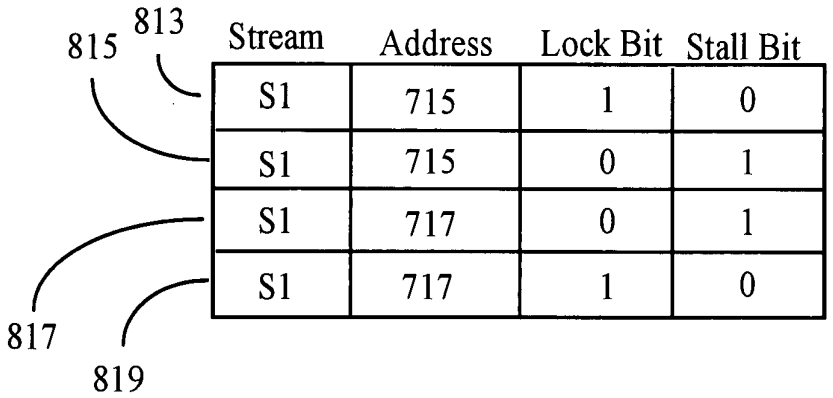


| Stream | Address | Lock Bit | Stall Bit |
|---|---|---|---|
| S1 | 715 | 1 | 0 |
| S1 | 715 | 0 | 1 |
| S1 | 717 | 0 | 1 |
| S1 | 717 | 1 | 0 |

***Fig. 8 (Hardware Lock)***